IN THE SPECIFICATION

Please replace the paragraph at page 4, lines 6-15, with the following rewritten paragraph:

In the example of Figure 62, a source terminal (S) of the P-channel transistor 11a is designated as Vdd (power supply potential) and a cathode of the EL element 15 is connected to ground potential (Vk). On the other hand, an anode is connected to a drain terminal (D) of the transistor [[11b]] 11a. Besides, a gate terminal of the P-channel transistor [[11a]] 11b is connected to a gate signal line 17a, a source terminal is connected to a source signal line 18, and a drain terminal is connected to the storage capacitance 19 and a gate terminal (G) of the P-channel transistor 11a.

Please replace the paragraph at page 8, lines 11-13, with the following rewritten paragraph:

the source driver circuit outputs the first current during the first period and outputs the ~~first~~ second current during the second period which comes after the first period.

Please replace the paragraph at page 39, line 7, with the following rewritten paragraph:

[[991]] 9991 Liquid crystal display panel

Please replace the paragraph at page 40, line 18, to page 41, line 6, with the following rewritten paragraph:

Some parts of drawings herein are omitted and/or enlarged/reduced herein for ease of understanding and/or illustration. For example, in a sectional view of a display panel shown in Figure 11, a encapsulation film 111 and the like are shown as being fairly thick. On the

other hand, in Figure 10, a sealing lid 85 is shown as being thin. Some parts are omitted. For example, although the display panel according to the present invention requires a polarizing plate [[of]] with a phase film such as a circular polarizing plate to prevent reflection, the phase film is omitted in drawings herein. This also applies to the drawings below. Besides, the same or similar forms, materials, functions, or operations are denoted by the same reference numbers or characters.

Please replace the paragraph at page 45, lines 12-22, with the following rewritten paragraph:

Desirably, film thickness of the thin film 111 is such that n·d is equal to or less than main emission wavelength λ of the EL element 15 (where n is the refraction factor of the thin film~~, or the sum of refraction factors~~ and d is the film thickness of the thin film; if two or more thin films are laminated, [[(]]n·d of each thin film is calculated[[)]] and the results are summed)~~; d is the film thickness of the thin film, or the sum of refraction factors if two or more thin films are laminated)~~. By satisfying this condition, it is possible to more than double the efficiency of light extraction from the EL element 15 compared to when a glass substrate is used for sealing. Also, an alloy, mixture, or laminate of aluminum and silver may be used.

Please replace the paragraph at page 45, line 23, to page 46, line 17, with the following rewritten paragraph:

A technique which uses an encapsulation film 111 for sealing instead of a sealing lid 85 as described above is called thin film encapsulation. In the case of "underside extraction (see Figure 10; light is extracted in the direction of the arrow in Figure 10)" in which light is extracted from the side of the board 71, thin film encapsulation involves forming an EL film

and then forming an aluminum electrode which will serve as a cathode on the EL film. Then, a resin layer is formed as a cushioning layer on the aluminum layer. An organic material such as acrylic or epoxy may be used for a cushioning layer. Suitable film thickness is from 1 μm to 10 μm (both inclusive). More preferably, the film thickness is from 2 μm to 6 μm (both inclusive). The encapsulation film [[74]] 111 is formed on the cushioning film (film layer). Without the cushioning film, structure of the EL film would be deformed by stress, resulting in streaky defects. As described above, the encapsulation film 111 may be made, for example, of DLC (diamond-like carbon) or an electrolytic capacitor of a laminar structure (structure consisting of thin dielectric films and aluminum films vapor-deposited alternately).

Please replace the paragraph at page 47, lines 3-10, with the following rewritten paragraph:

Half the light produced by the organic EL layer 15 is reflected by the reflective film 106 and emitted through the array board 71. However, the reflective film 106 reflects extraneous light, resulting in glare, which lowers display contrast. To deal with this situation, a $\lambda/4$ phase plate 108 and polarizing plate (polarizing film) 109 are placed on the array board 71. These are generally called circular polarizing plates (circular polarizing sheets).

Please replace the paragraph at page 50, lines 9-15, with the following rewritten paragraph:

To increase the quantity of light emitted from the board 71 to the outside, it is recommended to form a diffraction grating illustrated in Figure 69. The light produced by the EL layers 15 is diffracted by the diffraction grating, reducing the amount of light reflected at the ~~full~~ critical angle. This increases the amount of light emitted from the board 71, achieving a high-brightness display.

Please replace the paragraph at page 62, lines 14-22, with the following rewritten paragraph:

The source signal lines 18, through which minute current flows, are in a high-impedance state. To measure changes (or their absolute values) in the potential of the source signal lines 18 properly in this state, a high-impedance circuit (a positive input terminal of an input operational amplifier consisting of a FET circuit) is connected to each source signal line 18. That is, the probes 997 are electrically connected with the positive input ~~circuits~~ terminals of the input operational amplifiers (not shown) of the respective input circuits 993.

Please replace the paragraph at page 67, lines 5-9, with the following rewritten paragraph:

To speed up checking, a plurality of gate signal lines [[18]] 17a can be selected, approximate defect locations and defect mode can be detected, and then a turn-on voltage can be applied to each gate signal line 17a in a portion having defects in sequence to identify the defect locations and defect state.

Please replace the paragraph at page 67, lines 10-18, with the following rewritten paragraph:

The checking method according to the present invention does not require that all the source signal lines 18 should be probed at once. For example, the checking method according to the present invention may be performed by connecting probes 997 to the terminal electrodes 996 of the odd-numbered source signal lines [[18a]] 18b with the even-numbered source signal lines [[18b]] 18a kept open, and then by connecting probes 997 to the

terminal electrodes 996 of the even-numbered source signal lines 18a with the odd-numbered source signal lines 18b kept open.

Please replace the paragraph at page 67, lines 21-25, with the following rewritten paragraph:

Incidentally, although the gate driver circuit 12 in Figure 90 and the like is a built in type (other than an external semiconductor chip), this is not restrictive. The gate driver IC 12 may be constructed of a semiconductor chip and mounted on the ~~gate signal lines 17~~ array board 71 using a COG process.

Please replace the paragraph at page 71, line 20, to page 72, line 6, with the following rewritten paragraph:

Incidentally, the gate of the transistor 11a and gate of the transistor 11c are connected to the same gate signal line [[11a]] 17a. However, the gate of the transistor 11a and gate of the transistor 11c may be connected to different gate signal lines 17 (see Figure 32). Then, one pixel will have three gate signal lines (gate signal lines 17a, 17b, and 17c) (two gate signal lines 17a and 17b in the configuration in Figure 1). By controlling ON/OFF timing of the gate of the transistor 11b and ON/OFF timing of the gate of the transistor 11c separately, it is possible to further reduce variations in the current value of the EL element 15 due to variations in the transistor 11a.

Please replace the paragraph at page 73, line 20, to page 74, line 5, with the following rewritten paragraph:

This configuration makes it possible to pass minute current from the driver transistor 11a through the EL element 15 accurately. Also, by controlling the voltage applied to the

gate terminal of the transistor 11e (applied to the gate signal line [[11f]] 17f), it is possible to vary conditions of current output from the driver transistor 11a. Incidentally, the same voltage as the voltage applied to the gate signal line 17f is applied to the pixels in the display area. Of course, it is possible to form a gate driver circuit 12, which drives the gate signal line 17f, and apply an ac signal to the gate signal line 17f by operating the gate driver circuit 12.

Please replace the paragraph at page 74, lines 6-11, with the following rewritten paragraph:

Incidentally, gate signal line 17a, gate signal line 17b, and gate signal line [[1f]] 17f may be driven by different gate driver circuits or by a single gate driver circuit 12 as shown in Figure 2. The other part of the configuration is the same as that shown in Figure 1, and thus description thereof will be omitted.

Please replace the paragraph at page 78, lines 6-16, with the following rewritten paragraph:

Preferably, the transistors 11 of the pixels are polysilicon transistors formed by laser recrystallization (laser annealing) and the channel directions of all the transistors coincide with the direction of laser emission. In particular, it is preferable that the direction of laser emission coincides with the formation direction of the source signal lines [[14]] 18. This will make the characteristics of the driver transistors 11a along the source signal lines [[14]] 18 uniform and reduce amplitude fluctuations of the source signal lines [[14]] 18 during current programming. Reduced amplitudes make it possible to perform current programming accurately.

Please replace the paragraph at page 87, lines 4-13, with the following rewritten paragraph:

According to the present invention, the source driver circuit 14 is made of a semiconductor silicon chip and connected with a terminal on the source signal line 18 of the board 71 by ~~glass-on-chip~~ chip-on-glass (COG) technology. Metals such as chromium, copper, aluminum, and silver are used for wiring of signal lines such as the source signal lines 18. These metals provide low resistance with thin wiring width. If pixels are a reflective type, preferably the wiring is formed of the same material as reflecting films simultaneously with the reflecting films. This will simplify production processes.

Please replace the paragraph at page 89, lines 3-12, with the following rewritten paragraph:

The same applies to cases in which the source driver circuit 14 is formed on the board 71 by polysilicon technology such as low-temperature polysilicon technology. A plurality of inverter circuits are formed between an analog switching gate such as a transfer gate which drives the source signal line 18 and the shift register of the source driver circuit 14. The following matters (shift register output and output stages which drive signal lines (inverter circuits placed between output stages such as output gates or transfer gates)) are common to the gate driver circuit and source driver circuit.

Please replace the paragraph at page 92, lines 4-15, with the following rewritten paragraph:

Also, by using P-channel for the driver transistors (transistor 11a in Figure 1) which supply current to the EL element 15, it is possible to use a solid electrode made of thin metal film as the cathode of the EL elements 15. Also, current can be passed from the anode

potential Vdd to the EL elements 15 in the forward direction. In view of the above circumstances, it is preferable that the transistors in the pixels 16 and gate driver circuits 12 are P-channel. Thus, the use of P-channel transistors as the transistors (driver transistors and ~~itching~~ switching transistors) in the pixels 16 and gate driver circuits 12 according to the present invention is not merely a design matter.

Please replace the paragraph at page 100, lines 17-22, with the following rewritten paragraph:

Figure 170 shows state of voltage outputted to the gate signal lines 17b in the drive mode in Figure 168(b). As illustrated in Figure [[120]] 170, the gate signal lines 17b(1) to 17b(4) have the same waveforms as the gate signal lines 17b(5) to 17b(8). That is, the same operation is performed for each 4-pixel-row set.

Please replace the paragraph at page 103, lines 15-24, with the following rewritten paragraph:

With the drive method in Figure 168(a), the durations for which Vgl (turn-on voltage) occurs symmetrically during a period of 1 H get shorter as illustrated in Figure 171. In (a) of Figure 171, Vgl (turn-on voltage) is outputted for an entire period of 1 H (however, with the p-channel gate driver circuit 12 shown in Figure 113, it is not possible to produce a low-level output over the entire period of 1 H). A period of the Vgh voltage (turn-off voltage) occurs between 1 H and the next 1 H. However, this is shown in (a) of Figure [[1721]] 171 for ease of explanation.

Please replace the paragraph at page 104, lines 7-15, with the following rewritten paragraph:

With the drive method in Figure 168(b), the durations for which Vgl (turn-on voltage) occurs symmetrically during a period of 2 Hs get shorter as illustrated in Figure 172. In (a) of Figure 172, Vgl (turn-on voltage) is outputted for an entire period of [[1 H]] 2 H (however, with the p-channel gate driver circuit 12 shown in Figure 113, it is not possible to produce a low-level output over the entire period of 2 Hs). A period of the Vgh voltage (turn-off voltage) occurs between 2 Hs and the next 2 Hs. This is similar to the case with Figure 171.

Please replace the paragraph at page 109, lines 6-20, with the following rewritten paragraph:

In Figure 174, again it is possible to adjust (vary) the brightness of the screen 50 by varying the number of illuminated pixel rows (the number of displayed pixel rows 53 can be varied or adjusted as in the case of Figure 168). Also, by varying the ratio of a black insertion area (area B in Figure 174), it is possible to achieve an optimum state according to image display condition. For example, in the case of still pictures, it is necessary to avoid increasing area B. Increasing area B will cause flickering. In the case of still pictures, the display area 53 should be scattered in the screen 50. For example, a QCIF panel has 220 pixel rows. To display a still picture using 55 pixel rows, since [[220/44]] 220/55 = 4, one in every four pixel rows can be displayed. To display 10 pixel rows out of the 200 pixel rows, one in every 22 pixel rows (220/10 = 22) can be displayed.

Please replace the paragraph at page 112, line 19, to page 113, line 6, with the following rewritten paragraph:

Figure 177 shows output waveforms of gate signal lines 17b in the case where the drive system in Figure 174(a) is used. With the pixel configuration in Figure 1, on/off signals (Vgh is a turn-off voltage and Vgl is a turn-on voltage) applied to the gate signal lines 17b turn on and off the transistors 11d, thereby turning on and off the EL elements 15. In Figure [[1]] 177, the top row contains the horizontal scanning period, where symbol L represents the number of pixel rows (in the case of a QCIF panel, L = 220 pixel rows). In Figures 168 and 174, again the drive systems according to the present invention are not limited to the pixel configuration in Figure 1. Needless to say, they may also be applied to other pixel configurations (e.g., Figure 38).

Please replace the paragraph at page 117, line 16, to page 118, line 14, with the following rewritten paragraph:

Incidentally, the words "images are written" and "images are displayed" are used in Figures 179(a) and (c), and basically the present invention is characterized in that images are displayed (illuminated). Thus, writing an image (running a program) does not need to be identical with displaying an image. That is, one may think that in Figures 179(a) and (c), by controlling the gate signal lines 17b, the present invention controls the current flowing through the EL elements 15, and thereby puts images into illumination or non-illumination mode. Thus, it is possible to switch between the state in Figure 179(a) and state in Figure 179(b) at once (e.g., in a period of 1 H). For example, this can be done through control of an enable terminal (on-state and off-state are held in the shift registers of the gate driver circuit 12b (in Figure 179(a), the shift register for the even-numbered pixel rows holds on-state data) and the states in Figures 179(b) and (d) are displayed when the enable terminal is off and the

state in Figure 179(a) is displayed when the enable terminal is on). Thus, the displays in Figures 179(a) and 179(c) can be achieved using on-state and off-state of the gate signal lines 17b (image data is held in the capacitor 19 beforehand in the case of the pixel configuration in Figure 1, for example). It has been stated that each of the modes in Figures 179(a), (b), (c), and (d) occurs for one [[1]] frame period.

Please replace the paragraph at page 118, line 15, to page 119, line 20, with the following rewritten paragraph:

However, the present invention is not limited to these display modes. To improve at least movie display condition, black insertion mode such as the one shown in Figures 179(b) or (d) can be run for 4 msec. Thus, in the example of the present invention, the display modes in Figures 179(a) and (c) can be brought about not only by scanning the gate signal lines 17b using the shift register circuits of the gate driver circuit 12b. These modes can be brought about by mutually connecting odd-numbered gate signal lines 17b (referred to as an odd-numbered gate signal line group), mutually connecting even-numbered gate signal lines 17b (referred to as an even-numbered gate signal line group), and applying turn-on and turn-off voltages alternately to the odd-numbered gate signal line group and even-numbered gate signal line group. The display mode in Figure 179(c) is brought about if a turn-on voltage is applied to the odd-numbered gate signal line group and a turn-off voltage is applied to the even-numbered gate signal line group. The display mode in Figure 179(a) is brought about if a turn-on voltage is applied to the even-numbered gate signal line group and a turn-off voltage is applied to the odd-numbered gate signal line group. The display modes in Figures 179(b) and (d) are brought about if a turn-off voltage is applied to both odd-numbered gate signal line group and even-numbered gate signal line group. Each of the modes in Figures [[129]] 179(a), (b), (c), and (d) (especially Figures 179(b) and (d)) should be brought about

for 4 msec or longer. The drive system in Figure 179 alternates between screen display mode (Figures 179(a) and (c)) and black display mode (black insertion, Figures 179(b) and (d)). This makes image display intermittent, improving movie display performance (without blurred moving pictures).

Please replace the paragraph at page 142, line 24, to page 143, line 6, with the following rewritten paragraph:

For example, a tenfold increase in the output current from the source driver IC 14 results in a tenfold increase in the current programmed into the pixel 16. This results in a tenfold increase in the emission brightness of the EL element 15 as well. Thus, to obtain predetermined brightness, a light emission period is reduced tenfold by reducing the conduction period (ON time) of the transistor [[17d]] 11d in Figure 1 tenfold compared to a conventional conduction period.

Please replace the paragraph at page 154, lines 6-16, with the following rewritten paragraph:

In Figure 15, a gate signal line 17a(1) is selected (Vgl voltage) and a programming current flows through the source signal line 18 in the direction from the transistor 11a in the selected pixel row to the source driver circuit 14. Incidentally, the direction in which the programming current flows varies with the pixel configuration. If the driver transistor 11a of the pixel 16 is a p-channel transistor, the programming current Iw flows form the pixel 16 to the source driver circuit [[16]] 14. If the driver transistor 11a of the pixel 16 is an n-channel transistor, the programming current Iw flows form the source driver circuit 16 to the pixel [[16]] 14.

Please replace the paragraph at page 164, line 19, to page 165, line 6, with the following rewritten paragraph:

To deal with this problem, preferably a write pixel row 51 is sandwiched by non-display areas [[53]] 52 as illustrated in Figure 66. It is preferable to program the write pixel row with current (voltage), apply a turn-on voltage to the gate signal line 17b of the pixel row after one horizontal scanning period, and thereby pass current through the EL element 15. Preferably, a turn-off voltage is applied to the gate signal line 17b of each pixel row at least 3 μsec after applying a turn-on voltage to the gate signal line 17a which selects the pixel row. Preferably, the pixel rows before and after the write pixel rows 51 are included in the non-display area 52 as illustrated in Figure 66 if there is no restriction on the timing to pass current through the EL element 15.

Please replace the paragraph at page 170, line 19, to page 171, line 8, with the following rewritten paragraph:

It is important to maintain the terminal voltage of the capacitor 19 programmed with current or voltage. This is because [[if]] any change (charge/discharge) in the terminal voltage of the capacitor 19 ~~changes (charge/discharge)~~ during one field (frame) period causes changes in the screen brightness, resulting in flickering at lower frame rates~~, flickering occurs when the screen brightness changes and the frame rate lowers~~. The current passed through the EL element 15 by the transistor 11a must be higher than 65%. More specifically, if the initial current written into the pixel 16 and passed through the EL element 15 is taken as 100%, the current passed through the EL element 15 just before it is written into the pixel 16 in the next frame (field) must not fall below 65%. The capacitance of the capacitor 19 and turn-off characteristics of the voltage-holding transistor 11b are determined in such a way as to satisfy the above conditions.

Please replace the paragraph at page 174, lines 1-12, with the following rewritten paragraph:

If the brightness of the display area 53 is kept at a predetermined value, the larger the display area 53, the brighter the display screen 50. For example, when the brightness of the image display area 53 is 100 (nt), if the percentage of the display screen 50 accounted for by the display area 53 changes from 10% to 20%, the brightness of the screen is doubled. Thus, by varying the proportion of the display area 53 in the entire screen 50, it is possible to vary the display brightness of the screen. The present invention provides a system which controls image display by controlling the size of the display area [[52]] 53 with respect to the display 50.

Please replace the paragraph at page 174, line 13, to page 175, line 6, with the following rewritten paragraph:

The size of the display area 53 can be specified freely by controlling data pulses (ST2) sent to the shift register circuit 61 (See Figure 6). Also, by varying the input timing and period of the data pulses, it is possible to switch between the display condition shown in Figure 16 and display condition shown in Figure 13 (the size of the non-display area 52 is made different between Figure 13 and Figure 16 for ease of explanation). If the sizes of the non-display areas 52 are made equal, the same brightness can be obtained (provided the same reference current are applied to the source driver IC (described later)). Increasing the number of data pulses in one 1 F period thereby extending the display area [[52]] 53 makes the screen 50 brighter and decreasing it makes the screen 50 dimmer. Also, continuous application of the data pulses brings on the display condition shown in Figure 13 while intermittent input of the data pulses brings on the display condition shown in Figure 16. Thus, the brightness of

image display can be controlled easily by simply controlling the data pulses applied to the shift registers 61.

Please replace the paragraph at page 210, line 20, to page 211, line 8, with the following rewritten paragraph:

As shown in Figure 30, when the write pixel row is the (1)-th pixel row (see the 1H column in Figure [[30]] 31), the gate signal lines 17a(1), (2), (3), (4), and (5) are selected (in the case of configuration shown in Figure 1). That is, the switching transistors 11b and the transistors 11c in the pixel rows (1), (2), (3), (4), and (5) are on. Besides, since ISEL is low, the current output circuit A which outputs 25 times larger current is selected and connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b. Thus, the switching transistors 11d in the pixel rows (1), (2), (3), (4), and (5) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Please replace the paragraph at page 213, lines 1-4, with the following rewritten paragraph:

Thus, each transistor 11a in the pixel row (1) deliver a current of Iw $\times$ 5 to the source signal line 18. Then, the capacitor 19 in ~~each~~ pixel row (1) is programmed with a 5 times larger current.

Please replace the paragraph at page 214, lines 3-23, with the following rewritten paragraph:

In the next 1/2 H period (1/2 of the horizontal scanning period), only the write pixel row 51a is selected. That is, only the (2)-th pixel row is selected. As can be seen from

Figure 31, a turn-on voltage (Vgl) is applied only to the gate signal line 17a(2) and a turn-off voltage (Vgh) is applied to the gate signal lines 17a (3), (4), (5), and (6). Thus, the transistors 11a in the pixel rows (1) and (2) are in operation (the pixel row (1) supplies current to the EL element 15 and the pixel row (2) supplies current to the source signal line 18), but the switching transistors 11b and the transistors 11c in the pixel rows (3), (4), (5), and (6) are off. That is, they are non-selected. Besides, since ISEL is high, the current output circuit B which outputs 5 times larger current is selected and the current output circuit ~~1222b~~ B is connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b, which is in the same state as during the first 1/2 H. Thus, the switching transistors 11d in the pixel rows (2), (3), (4), (5), and (6) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Please replace the paragraph at page 219, lines 10-25, with the following rewritten paragraph:

The N-fold pulse driving method according to the present invention mentioned above uses the same waveform for the gate signal lines 17b of different pixel rows and applies current by shifting the pixel rows at 1 H intervals. The use of such scanning makes it possible to shift illuminating pixel rows in sequence with the illumination duration of the EL elements 15 fixed to 1F/N. It is easy to shift pixel rows in this way while using the same waveform for the gate signal lines 17b of the pixel rows. It can be done by simply controlling data ST1 and ST2 applied to the shift register circuits 61a and 61b in Figure 6. For example, if Vg1 is output to the gate signal line 17b when input ST1 is low and Vgh is output to the gate signal line 17b when input ST1 is high, ST2 applied to the shift register

circuit [[17b]] 61b can be set low for a period of 1F/N and set high for the remaining period. Then, inputted ST2 can be shifted using a clock CLK2 synchronized with 1 H.

Please replace the paragraph at page 220, lines 1-12, with the following rewritten paragraph:

Incidentally, the EL elements 15 must be turned on and off at intervals of 0.5 msec or longer. Short intervals will lead to insufficient black display due to persistence of vision, resulting in blurred images and making it look as if the resolution has lowered. This also represents a display state of a data holding display. However, increasing the on/off intervals to 100 msec will cause flickering. Thus, the on/off intervals of the EL elements must be not shorter than 0.5 ~~μsec~~ msec and not longer than 100 msec. More preferably, the on/off intervals should be from 2 msec to 30 msec (both inclusive). Even more preferably, the on/off intervals should be from 3 msec to 20 msec (both inclusive).

Please replace the paragraph at page 220, line 20, to page 221, line 9, with the following rewritten paragraph:

Incidentally, it is preferable that the number of divisions of a black screen can be varied between still pictures and moving pictures. When N = 4, 75% is occupied by a black screen (non-display area 52) and 25% is occupied by image display (display area 53). When the number of divisions is 1, a strip of black display (non-display area 52) which makes up 75% is scanned vertically. When the number of divisions is 3, three blocks are scanned, where each block consists of a black screen which makes up 25% and a display screen which makes up 25/3 percent. The number of divisions is increased for still pictures and decreased for moving pictures. The switching can be done either automatically according to input

images (detection of moving pictures) or manually by the user. Alternatively, the switching can be done according to input ~~outlet~~ contents such as video on the display apparatus.

Please replace the paragraph at page 237, lines 4-15, with the following rewritten paragraph:

Thus, the gate signal line 17a is controlled by the gate driver circuit 12a while the gate signal line 17c is controlled by the gate driver circuit 12b. This makes it possible to freely specify the time to turn on the transistor 11b and reset the driver transistor 11a as well as the time to turn on the transistor [[111c]] 11c and program the driver transistor 11a with current. Other parts of the configuration are the same as or similar to those described in Figure 6, etc., and thus description thereof will be omitted. Incidentally, the gate driver circuits 12 are formed using polysilicon technology. Also, needless to say, the gate driver circuits 12a and 12b may be integrated into a single unit.

Please replace the paragraph at page 242, line 24, to page 243, line 8, with the following rewritten paragraph:

Similarly, if the shift register circuit 61a outputs a high-level signal third, a turn-on voltage is output to the gate signal lines 17c of the pixel 16(2), which now is in a state of being programmed with current (voltage). At the same time, a turn-on voltage is also output to the gate signal lines 17a of the pixel 16(3), turning on the transistor 11b of the pixel 16(3) and resetting the driver transistor 11a of the pixel 16(3). Thus, the gate signal lines 17a outputs turn-on voltages for a period of 2 Hs, and the gate signal lines 17c receive a turn-on voltage for a period of 1 H.

Please replace the paragraph at page 244, lines 3-22, with the following rewritten paragraph:

As shown in Figure 39(a), the transistors 11c and 11e are turned off and the transistor 11d is turned on. Then, the drain (D) terminal and gate (G) terminal of the current-programming transistor [[11b]] 11a are short-circuited and a current Ib flows between them as shown in the figure. Generally, the transistor 11b has been programmed with current in the previous field (frame) and is capable of passing current (this is natural because the gate potential is held in the capacitor 19 for a period of 1F and image is displayed. However, current does not flow during a completely black display). In this state, as the transistor 11e is turned off and the transistor 11d is turned on, the drive current Ib flows through the gate (G) terminal of the transistor 11a (gate (G) terminal and the drain (D) terminal are short-circuited). Consequently, the gate (G) terminal and drain (D) terminal of the transistor 11a have the same potential, resetting the transistor 11a (to a state in which no current flows). Since the driver transistor 11b shares a common gate (G) terminal with the current-programming transistor 11a, the driver transistor 11b is also reset.

Please replace the paragraph at page 245, line 23, to page 246, line 15, with the following rewritten paragraph:

As in the case of Figure 33(a), if the reset mode in Figure 39(a) is synchronized with the current-programming mode in Figure 39(b), there is no problem because the period from the reset mode in Figure 39(a) to the current-programming mode in Figure 39(b) is fixed (constant). That is, preferably the period from the reset mode in Figure 33(a) or Figure 39(a) to the current-programming mode in Figure 33(b) or Figure 39(b) should be from 1 H to 10 Hs (ten horizontal scanning periods) both inclusive. More preferably, it should be from 1 H to 5 Hs or from 20 μsec to 2 msec (both inclusive). If this period is short, the driver

transistors [[11]] 11a are not reset completely. If it is too long, the driver transistor 11 is turned off completely, which means that much time is required for current programming. Also, the brightness of the screen 50 is decreased. This is not necessarily true if black insertion is made (non-display area 52 is generated) as shown in Figure 13 because the black insertion (non-display area 52) is used for N-fold pulse driving.

Please replace the paragraph at page 247, lines 1-14, with the following rewritten paragraph:

If the programming current Iw is 0 A (black display), the transistor 11b is held in the state in Figure ~~33(a)~~ 39(a) in which it does not pass current, and thus proper black display is achieved. Also, when performing current programming for white display in Figure 39(b), the current programming is started from offset voltage of completely black display even if there are variations in the characteristics of driver transistors in pixels (the offset voltage is a starting voltage at which a current specified according to the characteristics of each driver transistor starts to flow). Thus, the time required to reach a target current value becomes uniform according to gradations. This eliminates gradation errors due to variations in the characteristics of the transistor 11a or 11b, making it possible to achieve proper image display.

Please replace the paragraph at page 254, lines 9-17, with the following rewritten paragraph:

As in the case of Figure 33(a), if the reset mode in Figure 44(a) is synchronized with the voltage-programming mode in Figure 44(b), there is no problem because the period from the reset mode in Figure 44(a) to the current-programming mode in Figure 44(b) is fixed (constant). If this period is short, the driver transistors 11 are not reset completely. If it is too

long, the driver transistor 11a is turned off completely, which means that much time is required for current programming. Also, the brightness of the screen [[12]] 50 is decreased.

Please replace the paragraph at page 255, line 23, to page 256, line 2, with the following rewritten paragraph:

After the ~~current~~ voltage programming in Figure 44(b), the transistor 11d is turned off and the transistor 11d is turned on to deliver the programming current to the EL element 15 from the driver transistor 11a, and thereby illuminate the EL element 15, as shown in Figure 44(c).

Please replace the paragraph at page 258, lines 17-23, with the following rewritten paragraph:

Thus, in the case of a QCIF display panel, which has 220 vertical scanning lines, at least 220/5 = 44 or more lines should be grouped into a block. More preferably, 220/10 = [[11]] 22 or more lines should be grouped into a block. However, if odd-numbered rows and even-numbered rows are grouped into two different blocks, there is not much flickering even at a low frame rate, and thus the two blocks are sufficient.

Please replace the paragraph at page 259, lines 6-14, with the following rewritten paragraph:

Incidentally, in the example in Figure 40, the gate signal lines 17b do not intersect the illumination control lines 401. Thus, there can be no defect in which a gate signal line 17b would become short-circuited with an illumination control line 401. Also, since there is no capacitive coupling between gate signal lines 17b and illumination control lines 401, ~~addition of capacitance~~ capacitive load is very small when the gate signal lines 17b are viewed from

the illumination control lines 401. This makes it easy to drive the illumination control lines 401.

Please replace the paragraph at page 261, lines 6-9, with the following rewritten paragraph:

In the above example, one ~~selection pixel row~~ selection gate signal line is placed (formed) per pixel row. The present invention is not limited to this and a selection gate signal line may be placed (formed) for two or more pixel rows.

Please replace the paragraph at page 264, line 17, to page 265, line 6, with the following rewritten paragraph:

Besides, it is useful to increase penetration voltage by intentionally forming a capacitor 19b between the gate signal line 17a and the gate (G) terminal of the transistor 11a (see Figure 42(a)). Preferably, the capacitance of the capacitor 19b is between 1/50 and 1/10 (both inclusive) of the capacitance of a normal capacitor 19a. More preferably, it is between 1/40 and 1/15 (both inclusive). Alternatively, it should be from 1 to 10 times (both inclusive) the source-gate (or source-drain [[(SG)]] (SD) or gate-drain (GD)) capacitance of the transistor 11b. More preferably, it is from 2 to 6 times (both inclusive) the SG capacitance. Incidentally, the capacitor 19b may be formed or placed between one terminal of the capacitor 19a (gate (G) terminal of the transistor 11a) and source (S) terminal of the transistor 11d. In that case, the capacitance and the like have the same values as those described above.

Please replace the paragraph at page 265, line 22, to page 266, line 3, with the following rewritten paragraph:

The transistor 11b should be a p-channel transistor and should have at least two gates. Preferably, it has three or more gates. More preferably, it has four or more gates. Capacitors with a capacitance of 1 to 10 times the source-gate ([[SG]] SD or gate-drain (GD)) capacitance of the transistor 11b (when activated) are placed or formed in series.

Please replace the paragraph at page 268, line 14, to page 269, line 5, with the following rewritten paragraph:

Preferably, the size (capacitance) of the penetration-voltage generating capacitors 19b is varied among R, G, and B, which make pixels modulated. This is because drive current varies among the EL elements 15 of R, G, and B as well as because cutoff voltage varies with the EL element 15, varying the voltage (current) programmed into the gate (G) terminal of the driver transistor 11a among the EL elements 15. For example, if a capacitor [[11bR]] 19bR for the R pixel is 0.02 pF, capacitors [[11bG]] 19bG and [[11bB]] 19bB for the other colors (G and B pixels) should be 0.025 pF. Also, if the capacitor [[11bR]] 19bR for the R pixel is 0.02 pF, the capacitor [[11bG]] 19bG for the G pixel should be 0.03 pF and the capacitor [[11bB]] 19bB for the B pixel should be 0.025 pF, for example. By varying the capacitance of the capacitors [[11b]] 19b among the R, G, and B pixels in this way, it is possible to adjust offset drive current separately for R, G, and B. This makes it possible to optimize black display levels for R, G, and B.

Please replace the paragraph at page 286, line 24, to page 287, line 8, with the following rewritten paragraph:

The horizontal axis represents the ratio of the product of the reverse bias voltage Vm and its application duration t1 in a period to a rated terminal voltage V0. For example, if the reverse bias voltage Vm is applied at 60 Hz (60 Hz has no particular meaning) for 1/2 (half) a period, then t1 = 0.5. Further, t2 is the application duration of the rated terminal voltage. Also, if the terminal voltage (rated terminal voltage) is 8 V when a current with a current density of 100 A per square meter is applied at time 0 (zero) and if the reverse bias voltage Vm is [[8 V]] -8V, then |reverse bias voltage × t1|/(rated terminal voltage × t2) = |-8 (V) × 0.5|/(8 (V) × 0.5) = 1.0.

Please replace the paragraph at page 293, line 19, to page 294, line 6, with the following rewritten paragraph:

In the next 1 H (horizontal scanning period), a turn-off voltage (Vgh) is applied to the gate signal line 17a, and the second pixel row is selected. That is, a turn-on voltage is applied to a gate signal line 17b(2). On the other hand, a turn-on voltage (Vgl) is applied to the gate signal line 17b, the transistor 11d is turned on, and a current from the transistor 11a flows through the EL element 15, causing the EL element 15 to emit light. Also, a turn-off voltage [[(Vsh)]] (Vgh) is applied to the reverse bias line 471(1) stopping the reverse bias voltage from being applied to the EL elements 15 in the first pixel row (1). The voltage Vsl (reverse bias voltage) is applied to a reverse bias line 471(2) in the second pixel row.

Please replace the paragraph at page 297, lines 10-25, with the following rewritten paragraph:

For example, in the pixel configuration in Figure 1, the pixel 16 is selected (the transistors 11b and 11c are turned on) and a low voltage V0 (e.g., GND voltage) which the source driver IC (circuit) 14 can output is outputted from the source driver IC and applied to

the drain (D) terminal of the driver transistor 11a. If the transistor 11d is turned on as well in this state, the voltage V0 is applied to the anode terminal of the EL element. At the same time, if a voltage Vm lower than the voltage V0 by ~~-5 to -15~~ 5 to 15 V is applied to the cathode Vk of the EL element 15, a reverse bias voltage is applied to the EL element 15. Also, if a voltage lower than the voltage V0 by 0 to -5 V is applied as the Vdd voltage, the transistor 11a is turned off. Thus, by outputting a voltage from the source driver circuit 14 and thereby controlling the gate signal line 17, it is possible to apply a reverse bias voltage to the EL element 15.

Please replace the paragraph at page 302, lines 1-6, with the following rewritten paragraph:

To apply the reverse bias voltage Vm to the EL element 15, it is necessary to turn off the transistor 11a. To turn off the transistor 11a, the ~~Vdd~~ drain terminal and gate (G) terminal of the transistor 11a can be short-circuited. This configuration will be described with reference to Figure 53 later.

Please replace the paragraph at page 320, lines 3-12, with the following rewritten paragraph:

Off-leakage bright spots occur in black display. Off-leakage bright spots increase black illuminance (illuminance obtained by measuring the display screen of the display panel with an illuminance meter) (excessive brightness resulting in a whitish screen). Figure 121(a) shows a voltage waveform applied to a gate signal line 17b. The application duration of a turn-off voltage is denoted by C and one cycle of the applied turn-off voltage is denoted by [[C]] S. Incidentally, although it is assumed here that the cycle [[C]] S corresponds to a period of 1 H, this is not restrictive.

Please replace the paragraph at page 325, lines 10-22, with the following rewritten paragraph:

Referring to Figure 138, Gate Signal Line 17a(1) represents a signal waveform of the gate signal line 17a of a pixel (1). Gate Signal Line 17a(2) represents a signal waveform of the gate signal line 17a of a pixel (2) next to the pixel (1). Gate Signal Line 17a(3) represents a signal waveform of the gate signal line 17a of a pixel (3) next to the pixel (2). Source Signal Line 18 represents a voltage (current) waveform applied to the source signal line. The pixel potential illustrates a capacitor potential of the pixel (2) (voltage waveform of the gate terminal G of the driver transistor 11a). The gate signal lines 17a are scanned in the order: (1) → (2) → (3) → (4) → (5) → ... (1) → (2) → ....

Please replace the paragraph at page 339, lines 15-22, with the following rewritten paragraph:

In Figure 143, a capacitor driver 1431 generates square waves (referred to as source coupling signals. See Figure 144.), which are applied by coupling capacitors 1434 to the source signal lines 18. One end of each coupling capacitor [[1433]] 1434 is connected to a capacitor signal line 1433. The square waves are applied to the capacitor signal line 1433. The source coupling signals are applied to the source signal lines in sync with horizontal synchronization signals.

Please replace the paragraph at page 343, lines 7-18, with the following rewritten paragraph:

Source Signal Line 18 represents a voltage (current) waveform applied to the source signal line. The pixel potential (2) illustrates a capacitor potential of the pixel (2) (voltage

waveform of the gate terminal G of the driver transistor 11a). The gate signal lines 17a are scanned in the order: (1) → (2) → (3) → (4) → (5) → ... (1) → (2) → .... The common signal lines 1511 are also scanned in the order: (1) → (2) → (3) → (4) → (5) → ... (1) → (2) → .... For ease of explanation, description will be given with a focus on the pixel potential of the pixel (2) (the potential at the gate terminal G of the driver transistor 11a). First, image data of all the fields is held in the pixel 16.

Please replace the paragraph at page 345, lines 12-20, with the following rewritten paragraph:

As can be seen from the above operation, the penetration voltage caused by the parasitic capacitance 1381 and the like is compensated for by the application of a signal to the common signal line 1511. This compensation allows accurate current programming of the pixels 16. Incidentally, it has been stated that the potential of the common signal line 1511 changes from Vch to Vcl after a lapse of [[Ta]] Tb from the completion of 1 H. However, Tb may be either 0 sec. (immediately upon termination of 1 H) or 1 H or longer.

Please replace the paragraph at page 347, lines 10-16, with the following rewritten paragraph:

Source Signal Line 18 represents a voltage (current) waveform applied to the source signal line. The pixel potential (2) illustrates a capacitor potential of the pixel (2) (voltage waveform of the gate terminal G of the driver transistor 11a). The gate signal lines 17a are scanned in the order: (1) → (2) → (3) → (4) → (5) → ... (1) → (2) → ....

Please replace the paragraph at page 352, lines 6-14, with the following rewritten paragraph:

The above example compensates for the effect of penetration voltage through improvement or invention of a drive system. Penetration voltage can also be suppressed using pixel 16 configuration. In Figure [[146]] 148, a p-channel transistor [[11bn]] 11bp and n-channel transistor 11bn are used in place of the p-channel switching transistor 11b in Figure 1. They constitute an analog switch. An inverter 1481 is placed to turn on the p-channel transistor [[11bn]] 11bp and n-channel transistor 11bn simultaneously.

Please replace the paragraph at page 364, lines 1-9, with the following rewritten paragraph:

Incidentally, for ease of explanation, it is assumed that there are 63 current sources for a 6-bit configuration, but this is not restrictive. In the case of 8-bit configuration, 255 unit transistors 1854 can be formed (placed). For a 4-bit configuration, 15 unit transistors 1854 can be formed (placed). The transistors 1854 constituting the unit current sources have a channel width W and channel ~~width~~ length L. The use of equal transistors makes it possible to construct output stages with small variations.

Please replace the paragraph at page 382, lines 14-19, with the following rewritten paragraph:

To reduce voltage drops in the common anode lines [[832]] 833 and anode wires 834, it is recommended to form a common anode line [[832a]] 833a on the upper side of the display screen 50, form a common anode line [[832b]] 833b on the lower side of the display screen 50, and short-circuit the anode wires 834 at the top and bottom, as illustrated in Figure 84.

Please replace the paragraph at page 383, lines 3-19, with the following rewritten paragraph:

In the case of organic EL or other self-luminous elements, light produced by the EL elements 15 is reflected diffusely within the array board 71, causing intense light to be radiated from places other than the display area 50. To prevent or reduce the diffusely reflected light, it is preferable that light-absorbing films 1011 are formed in ineffective areas which do not pass light effective for image display. The light-absorbing films are formed on an outer surface of a sealing lid 85, inner surface of the sealing lid 85, side face of the ~~board 70~~ array board 71, area on the board other than the image display area (light-absorbing film 1011b), etc. Incidentally, instead of light-absorbing films, light-absorbing sheets or light-absorbing walls may be installed. Besides, the concept of light absorption also includes schemes or structures which diverge light by scattering it. In a broader sense, it also includes schemes or structures which confine light through reflection.

Please replace the paragraph at page 386, lines 3-9, with the following rewritten paragraph:

Although organic EL display apparatus are described herein, the display panels used for the organic EL display apparatus are not limited to organic EL display panels. For example, as illustrated in Figure 99, a display apparatus may be composed of an organic EL display panel used as a main display panel and a liquid crystal display panel [[991]] 9991 used as a sub display panel.

Please replace the paragraph at page 386, line 20, to page 387, line 4, with the following rewritten paragraph:

Reference numeral 1004 denotes a polarizing plate or circular polarizing plate. A dispersing agent 1003 is placed or formed between the polarizing plates 1004 and array boards 71. The dispersing agent 1003 also functions as an adhesive which bonds the polarizing plates 1004 and array boards 71 together. The dispersing agent [[1004]] 1003 may be, for example, an acrylic adhesive containing fine-powdered titanium oxide or an acrylic adhesive containing fine-powdered calcium carbonate The dispersing agent [[1004]] 1003 improves the efficiency of extracting light produced by the EL elements 15.

Please replace the paragraph at page 390, lines 11-19, with the following rewritten paragraph:

In addition to a push switch, the key 572 may be a slide switch or other mechanical switch. Speech recognition may also be used for switching. For example, the switch may be configured such that display colors on the display screen 50 of the display panel will change as the user ~~speaks a phrase~~ enters a color change command by speaking such as "high-definition display," "256-color mode," or "low-color display mode" into the phone. This can be implemented easily using existing speech recognition technology.